



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,374	12/12/2001	Kwang Seok Oh	W2K1070	2810
23513	7590	05/10/2005	EXAMINER	
GUNNISON MCKAY & HODGSON, LLP GARDEN WEST OFFICE PLAZA, SUITE 220 1900 GARDEN ROAD MONTEREY, CA 93940			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/015,374

6

Applicant(s)

OH ET AL.

Examiner

Alexander O. Williams

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21,22,39-47 and 50-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21,22,39-47 and 50-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Art Unit: 2826

Serial Number: 10/015374 Attorney's Docket #: BK-0005

Filing Date: 12/12/01; claimed foreign priority to 3/9/2001

Applicant: Oh et al.

Applicant's Amendment filed 3/10/05 has been acknowledged.

Claims 1-20, 23-38, 48, 49 and 65 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C.

§ 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21, 22, 53 to 59, 63 and 64 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ball (U.S. Patent # 5,689,135).

21. Ball (figures 1 to 5) specifically figure 1 show a semiconductor package **10** comprising: a first semiconductor chip **12** having opposed first and second surfaces, the second surface including a plurality of pads **18**; an adhesive layer **20** coupled to the second surface of the first semiconductor chip; and a second semiconductor chip **14** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and an insulator **30** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is coupled between the first surface of the second semiconductor chip and the adhesive layer, and is vertically between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip.

22. A semiconductor package in accordance with Claim 21, Ball further comprising: at least one pad formed on the second surface of the first semiconductor chip; at least one first conductive wire **26** connecting the at least one pad of the first semiconductor chip and a substrate **16**; at least one pad **38** formed on the second surface of the second semiconductor chip; and at least one second conductive wire **36** connecting the at least one pad of the second semiconductor chip and the substrate.

53. Ball (figures 1 to 5) specifically figure 1 show a semiconductor package **10** comprising: a first semiconductor chip **12** having opposed first and

Art Unit: 2826

second surfaces; an adhesive layer **20** coupled to the second surface of the first semiconductor chip; a second semiconductor chip **14** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and an insulator **30** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip.

54. A semiconductor package in accordance with Claim 53, Ball further comprising: at least one pad **18** formed on the second surface of the first semiconductor chip; and at least one first conductive wire **26** connecting the at least one pad of the first semiconductor chip and a substrate **2**.

55. A semiconductor package in accordance with Claim 54, Ball further comprising: at least one pad **38** formed on the second surface of the second semiconductor chip; and at least one second conductive wire **36** connecting the at least one pad (inherit) of the second semiconductor chip and the substrate.

56. A semiconductor package in accordance with Claim 55, Ball show wherein the first semiconductor chip is an edge pad type semiconductor chip in which the at least one pad of the first semiconductor chip is formed at an inner circumference of the second surface.

57. A semiconductor package in accordance with Claim 55, Ball show wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

58. A semiconductor package in accordance with Claim 55, Ball show wherein the adhesive layer covers a part of the at least one first conductive wire positioned on the at least one pad of the first semiconductor chip.

59. A semiconductor package in accordance with Claim 55, Ball show wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

63. A semiconductor package in accordance with Claim 55, Ball show wherein a section of the at least one first conductive wires **26** is contacted with the insulator **30**.

64. A semiconductor package in accordance with Claim 53, Ball further comprising a sealing material **42** covering the first and second semiconductor chips, wherein a portion of the sealing material is between the second surface of the first semiconductor chip and the insulator.

Initially, and with respect to claims 43 to 46 and 60 to 62, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on an insulator and an adhesive layer deals

Art Unit: 2826

with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 21, 39, 42 to 47, 53, 54 and 64 are rejected under 35 U.S.C.

§ 103(a) as being unpatentable over by Pai et al. (U.S. Patent # 6,503,776 B2).

In claim 21, Pai et al. (figures 1 to 10) specifically figure 8 show a semiconductor package comprising: a first semiconductor chip 110 having opposed first and second surfaces; an adhesive layer 162 coupled to the second surface of the first semiconductor chip; a second semiconductor chip 130 stacked over the second surface of the first semiconductor chip and having

Art Unit: 2826

opposed first and second surfaces; and an insulator **162** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the first surface of the second semiconductor chip and the adhesive layer, and is vertically between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip.

39. Pai et al. (figures 1 to 10) specifically figure 8 show a semiconductor package comprising: a substrate **120**; a first semiconductor chip **110** coupled to the substrate, the first semiconductor chip having opposed first and second surfaces; a second semiconductor chip **130** having opposed first and second surfaces; a first means **160** coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip in a stack; at least one pad (shown, but not labeled on the surface of 110) formed on the second surface of the first semiconductor chip; and at least one first conductive wire **150** connecting the at least one pad of the first semiconductor chip and the substrate; at least one pad (shown but not labeled on the surface of 130) formed on the second surface of the second semiconductor chip; at least one second conductive wire **150** connecting the at least one pad of the second semiconductor chip and the substrate; and an insulator **166** coupled between the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire.

42. A semiconductor package in accordance with Claim 39, Pai et al. show wherein the insulator is one selected from a group consisting of: a

Art Unit: 2826

nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

47. A semiconductor package in accordance with Claim 39, Pai et al. further comprising a sealing material covering the substrate, the first and second semiconductor chips, and the at least one first and second conductive wires, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator (see figure 2).

53. Pai et al. (figures 1 to 10) specifically figure 8 show a semiconductor package comprising: a first semiconductor chip **110** having opposed first and second surfaces; an adhesive layer **162** coupled to the second surface of the first semiconductor chip; a second semiconductor chip **160** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and an insulator **162** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the adhesive layer and the first surface of the second semiconductor chip.

54. A semiconductor package in accordance with Claim 53, Pai et al. further comprising: at least one pad (not labeled, but shown on the surface of **110**) formed on the second surface of the first semiconductor chip; and at least one first conductive wire **150** connecting the at least one pad of the first semiconductor chip and a substrate **120**.

64. A semiconductor package in accordance with Claim 53, Pai et al. further comprising a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is between the second surface of the first semiconductor chip and the insulator (see figure 2).

Art Unit: 2826

As to claims 43 to 46, as to the grounds of rejection under section 103, see MPEP § 2113.

Therefore, it would have been obvious to one of ordinary skill in the art to use the adhesive and the insulator as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 21, 22, 39 to 47, 50 to 57 and 59 to 62 are rejected under 35 U.S.C. § 103(a) as being unpatentable over by Foster (U.S. Patent # 6,552,416 B1).

In claim 21, Foster (figures 1 to 10c) specifically figure 3B show a semiconductor package **10** comprising: a first semiconductor chip **30** having opposed first and second surfaces; an adhesive layer **33** coupled to the second surface of the first semiconductor chip; a second semiconductor chip **31** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and an insulator **33** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the first surface of the second semiconductor chip and the adhesive layer, and is vertically between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip.

22. A semiconductor package in accordance with Claim 21, Foster further comprising: at least one pad **34** formed on the second surface of the first semiconductor chip; at least one first conductive wire **35** connecting the at least one pad of the first semiconductor chip and a substrate; at least one pad **36** formed on the second surface of the second semiconductor chip; and at least one second conductive wire **35** connecting the at least one pad of the second semiconductor chip and the substrate.

39. Foster (figures 1 to 10c) specifically figure 3B show a semiconductor package comprising: a substrate **20**; a first semiconductor chip **30** coupled to the substrate, the first semiconductor chip having opposed first and second surfaces; a second semiconductor chip **31** having opposed first and second surfaces; a first means **33** coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip in a stack; at least one pad **34** formed on the second surface of the first semiconductor chip; and at least one first conductive wire **35** connecting the at least one pad of the first semiconductor chip and the substrate; at least one pad **36** formed on the second surface of the second semiconductor chip; at least one second conductive wire **35** connecting the at least one pad of the second semiconductor chip and the substrate; and an insulator **33** coupled between the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire.

40. A semiconductor package in accordance with Claim 39, Foster show wherein the first means **33** coupled to the second surface of the first semiconductor chip is an adhesive layer.

41. A semiconductor package in accordance with Claim 40, Foster show wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

42. A semiconductor package in accordance with Claim 39, Kondo et al. show wherein the insulator is one selected from a group consisting of: a

Art Unit: 2826

nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

42. A semiconductor package in accordance with Claim 39, Foster show wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, **a nonconductive adhesive tape/film**, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

47. A semiconductor package in accordance with Claim 39, Foster further comprising a sealing material **37** covering the substrate, the first and second semiconductor chips, and the at least one first and second conductive wires, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator.

50. Foster (figures 1 to 10c) specifically figure 3B show a semiconductor package **10** comprising: a first semiconductor chip **30** having opposed first and second surfaces, the second surface including a plurality of pads **34**; a plurality of conductive wires **35**, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip; a second semiconductor chip **31** stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads **36**; an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between each of the conductive wires and the first surface of the second semiconductor chip; an adhesive layer **33** attached the insulator and the second surface of the first semiconductor chip; and a sealing

material **37** covering the first and second semiconductor chips, wherein a portion of the sealing material is vertically between the pads of the second surface of the first semiconductor chip and the insulator.

51. Foster (figures 1 to 10c) specifically figure 3B show a semiconductor package **10** comprising: a first semiconductor chip **30** having opposed first and second surfaces, the second surface including a plurality of pads **34**; a plurality of conductive wires **35**, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip; a second semiconductor chip **31** stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads **36**; an insulator **33** coupled to the first surface of the second semiconductor chip, said insulator being between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip; and an adhesive layer **33** attached to the insulator and the second surface of the first semiconductor chip, the adhesive layer being entirely inward of the pads of the second surface of the first semiconductor chip.

52. A semiconductor package in accordance with Claim 51, Foster further comprising a sealing material **37** covering the first and second semiconductor chips, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator.

53. Foster (figures 1 to 10c) specifically figure 3B show a semiconductor package comprising: a first semiconductor chip **30** having opposed first and second surfaces; an adhesive layer **33** coupled to the second surface of the first

Art Unit: 2826

semiconductor chip; a second semiconductor chip **31** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and an insulator **33** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the adhesive layer and the first surface of the second semiconductor chip.

54. A semiconductor package in accordance with Claim 53, Foster further comprising: at least one pad **34** formed on the second surface of the first semiconductor chip; and at least one first conductive wire **35** connecting the at least one pad of the first semiconductor chip and a substrate **20**.

55. A semiconductor package in accordance with Claim 54, Foster further comprising: at least one pad **36** formed on the second surface of the second semiconductor chip; and at least one second conductive wire **35** connecting the at least one pad **36** of the second semiconductor chip **31** and the substrate **20**.

56. A semiconductor package in accordance with Claim 55, Foster show wherein the first semiconductor chip is an edge pad type semiconductor chip in which the at least one pad of the first semiconductor chip is formed at an inner circumference of the second surface.

57. A semiconductor package in accordance with Claim 55, Foster show wherein the adhesive layer **33** is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

59. A semiconductor package in accordance with Claim 55, Foster show wherein the insulator **33** is one selected from a group consisting of: a

Art Unit: 2826

nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

As to claims 43 to 46 and 60 to 62, as to the grounds of rejection under section 103, see MPEP § 2113.

Therefore, it would have been obvious to one of ordinary skill in the art to use the adhesive and the insulator as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 60 to 63 are rejected under 35 U.S.C. § 103(a) as being unpatentable over by Ball (U.S. Patent # 5,689,135).

60. A semiconductor package in accordance with Claim 55, Ball show wherein a first end of the at least one first conductive wire is bonded on the substrate by ball bonding and a second end of the at least one first conductive wire is bonded on the at least one pad of the first semiconductor chip by stitch bonding.

61. A semiconductor package in accordance with Claim 60, Ball show wherein a conductive ball is formed on the at least one pad of the first semiconductor chip bonded by the stitch bonding.

62. A semiconductor package in accordance with Claim 55, Ball show wherein a first end of the at least one first conductive wire is bonded on the substrate and a second end of the at least one first conductive wire is bonded on the at least one pad of the first semiconductor chip by stitch bonding.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 3/10/05 have been fully considered, but are not found to be persuasive in view of the outstanding and new grounds of rejections detailed above. The Examiner detailed the reasons for the outstanding rejection of at least claim 21 in a telephone interview on 5/2/05.

The insertion of Applicant's additional claimed language, for example, "in claims 21, 39, 50, 51 and 53" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Art Unit: 2826

Field of Search	Date
U.S. Class and subclass: 257/685,686,723,777,784,786	1/13/03 8/6/03 3/11/04 12/9/04 5/2/05
Other Documentation: foreign patents and literature in 257/685,686,723,777,784,786	1/13/03 8/6/03 3/11/04 12/9/04 5/2/05
Electronic data base(s): U.S. Patents	1/13/03 8/6/03 3/11/04 12/9/04 5/2/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
5/2/05



Alexander Williams
Primary Examiner